Eagle PCB Notes, started 2007-03-05, NerdFever.com

Last updated 2012-06-04 (Eagle v6.2.0 Light)

1 Introduction

This document records my notes for using Eagle PCB. Most of the text is my own, but there are places where I've cut-and-pasted information from the Eagle documentation or material found online.

This is not meant as a replacement for the Eagle documentation, but rather as commentary and interpretation.

I've been using BatchPCB.com to manufacture boards; their design rules influence some of the notes.

I find Eagle's user interface counter-intuitive in many ways. It's powerful, but the assumptions differ a lot from common GUI programs like MS Office and Photoshop. The fact that the manual is a poor translation from German doesn't help. So I have to refer to these notes to refresh my memory about how Eagle works after not using it for a while.

I make no promises that this material is accurate; I write what I learn but sometimes I may misunderstand. Feedback with corrections and improvements are welcome; please post them on NerdFever.com or email to dave@nerdfever.com.

2 Light version limits

- 2 layers
- 100 mm wide x 80 mm high
- One sheet
- Non-commercial

2.1 Personal standards

I find that 0805 parts are the smallest I can work with at all naked-eye. I can solder 0603 parts by hand, but only under a microscope.

Package grid

- 1 mm coarse, 0.05 mm fine
- Package outlines 0.127 mm (0.005"), in tPlace
- Text is 1.0 mm, 8% (0.5mm for tiny)
    - Old:
    - Package text is 0.04" width, 10%
    - Package outlines 0.005" in width

0805 footprint

- Nominal part is 2.0x1.25mm (up to 2.25x1.5mm)
- Pads are 1.0x1.5mm, spacing is 0.6mm (total length is 2.6mm)

2.2 Layer usage (personal)

- 1 Top | Top copper
- 16 Bottom | Bottom copper
- 17 Pads | Top & bottom copper
- 18 Vias | Top & bottom copper
- 19 Unrouted
- 20 Dimension | Top & bottom silkscreen
- 21 tPlace | Top silkscreen
- 22 bPlace | Bottom silkscreen
- 23 tOrigins
- 24 bOrigins
- 25 tNames | Top silkscreen
- 26 bNames | Bottom silkscreen
- 27 tValues
- 28 bValues
- 29 tStop | Top stop mask
- 30 bStop | Bottom stop mask
- 39/40 Keepout (packages)
- 41/42 Restrict (traces)
- 44 Drills (always plated-thru)
- 45 Holes (sometimes plated-thru, BatchPCB plates all holes)

2.3 Design rules

BatchPCB.com has the following requirements (as of 2009-10):

- 2 or 4 layer boards - 0.062" FR4 material
- 2 Layer sizing:
    - 8mil (~0.2 mm) spacing minimum
    - 8mil (~0.2 mm) traces minimum
    - 20mil (~0.5 mm) minimum drill size

- 4 Layer sizing:
    - 6mil (~0.15 mm) spacing minimum
    - 6mil (~0.15 mm) traces minimum
    - 13mil (~0.33 mm) minimum drill size
- No blind/buried vias
- 500mil (~12.7 mm) maximum drill size
- All drill hits are plated through
- No internal routes, no v-scoring, only drill files are sent to the fab house
- Board is routed to the indicated border (very clean edges)
- Soldermask both sides
- 1oz Copper
- No limit on the number of vias
- No limit on pads or components
- Multiple designs, multiple copies are allowed!
- Any size up to 10x15", measured in inch increments (254mm x 381mm)

3 My shortcut keys

These are defined in eagle.scr.

Key	Use
F1	Help
F2	Redraw window
F3	Fit window
F4	Change
F9	Value
F10	Name
F11	‘Grid inch 0.1 on; Grid alt inch 0.002;'
F12	'Grid mm 1 on; Grid alt mm 0.05';
^C	Cut (copy to paste buffer)
^D	Display (layers)
Alt-D	Display layers to appear on board
Ctl-Alt-D	Display all layers
^G	Group
^H	SmasH
^I	Info
^J	Junction
^K	MarK
^L	Layers
^M	Move
^N	Net
^P	Pinswap
^R	MirroR
^S	Show
^T	RotaTe
^U	RipUp
Alt-U	RipUp *
^V	Paste (from paste buffer)
^W	Wire (draw line)
^X	Delete
^Y	CopY part
^Z	Undo
Alt-Z	Redo
Alt-A	Display Airwires (unrouted)
Alt-T	Display Top layers of board
Alt-B	Display Bottom layers of board
Alt-K	Hide solder masK

4 Basic concepts

4.1 Schematics, boards, and devices

Eagle works with schematics, boards, and devices.

Devices are placed on the schematic, and connected with Nets. Then the Devices are placed on the board and routed with traces. Finally Gerber files are generated for delivery to the PCB fab house.

Boards have physical dimensions and multiple layers.

Schematics are checked using the Electrical Rule Check (ERC). Boards are checked with the Design Rule Check (DRC).

Devices are stored in Libraries. Each device consists of:

- Symbol(s) (for the schematic),
- Package(s) (board layout), and
- Connections between package pads and symbol pins

A given Device may have multiple Packages (for example both thru-hole and SMD versions); you choose which Package to use when adding a Device.

4.2 Editing – general (schematic, board, devices)

Selections

Selecting objects requires their origin be visible. The nearest origin will be selected. You can click Next to cycle to the next-closest, etc.

Only things present in the visible layers are selected. Make all layers visible if you want to manipulate them all.

Tools work on either individual objects/elements (default), or Groups (hold down Ctl while using command).

Clicking near the center of a line selects the whole line. Clicking near one end of a line selects the vertex.

To work with a group of objects

1. Choose Group tool
2. Drag rectangle around objects.
3. Chose tool (Move, etc.)
4. Either
    a. RIGHT-CLICK and use tool (drag, etc.)
    b. Ctrl-RIGHT-CLICK to use previously-selected tool on group

Cut, paste, copy, and delete

Cut copies selection into paste buffer when you press the Go button (traffic light icon). Cut does not delete anything (use Delete for that).

Copy duplicates the selected item(s).

Paste places a copy of the contents of the paste buffer.

To MOVE objects

1. Click MOVE
2. *Double-click* component, drag it into place
    a. First click selects
    b. Second click attaches device to mouse for dragging

Hold down **control** while selecting a move object to align it with the current grid.

Schematic/board synchronization

Forward/Backward annotation requires .brd/.sch to have the same name/directory, and to both be open while editing.

4.3 Design sequence

It helps a lot to do things in the right sequence; otherwise you'll end up having to go back and redo things.

1. Draw schematic & net it up. Create new/modified devices as needed.
2. Run ERC
3. Create new board, place parts (see 7.4 below). Run DRC.
4. Route (see 8.2 below). Run DRC again.
5. Place labels with 'text' in tPlace:
    a. PCB markings of signal names (match software & schematic)
    b. Mark on schematic and PCB which pins are to be removed for keying
    c. Mark JP pin positions by function
    d. Mark TP voltages (GND, 7.4v, 3.3v, etc.)
6. Generate gerber files, check in Viewplot or similar.
7. Upload to fab house.

See the sections below for details.

5 Schematic entry

5.1 Adding (inserting) devices into the schematic

Use command 'Add'. This adds from currently 'used' library. You can search from the current library(ies) in the search box at the bottom. Wildcards * and ? may be used (use '*term*' to start).

Say ‘USE *’ to load all libraries.

Say ‘USE -*’ to remove all libraries from ‘use’.

5.2 Connecting devices in the schematic

To draw wires (conductors) in the schematic use ‘Net’ tool (not ‘wire’).

Nets can be ‘named’ with the Name command (you can give signals names this way). You can make the names show up on the schematic with Label.

Start Nets from already named Nets to preserve the name and avoid the annoying dialog box.

Supply symbols & names

CMOS	**TTL**	**Name**	**Alt. Name**	**Symbol**	**Alt Symbol**
Vdd	Vcc	B+	+Supply	Up arrow	Circle
Vss	Vee	Circuit GND	Digital GND	Down triangle	Down arrow
		Earth GND	Analog GND	3-bar ground	2-bar gnd
		Chassis GND	Earth GND	bar 3 line gnd	1-bar gnd

See ‘Ground’ on Wikipedia.

Busses

Busses are a set of nets. They exist mainly to simplify schematics.

Busses are named according to which nets they include.

ERC errors and warnings

To find a coordinate – WINDOW x y

To find a net (will highlight it) – SHOW <name>. <name> can be either the name(s) of device(s) or net(s).

5.3 Important design tips

Digital outputs

Don’t forget weak pullups/pulldowns on safety-related output pins; you don’t want anything to go “bang” at initialization when the output pin is a floating input.

Digital inputs

Avoid floating inputs. CMOS floating inputs draw power. All floating inputs can toggle unpredictably.

Unused I/O pins

Set unused pins as:

- Outputs (usually tied to a power rail with 10k or so in series to limit current if set the wrong way), or,
- Inputs with a pullup/pulldown, or,
- Analog input (does not draw current on PIC32)

6 Working with device libraries

6.1 Creating devices

1. Create package – use 'name' to give pads NUMBERS (not names)
    a. Set grid to be ½ of smallest dimension you'll be working with
    b. Draw outline with 'wire' in tPlace
    c. Type 'smd' to create SMD pads (adjust size in box above)
    d. Use 'name' to give pads NUMBERS (not names)
    e. Draw in tKeepout and tRestrict as needed to keep components and traces out of any critical areas
2. Create symbol – use 'name' to give pins NAMES (not numbers)
    a. Usually stay with default 0.1 inch grid – just enough for adjacent pins
    b. Draw box with 'wire'
    c. Place pins with 'pin'
    d. Use 'name' to name pins
        i. If there are multiple pins with the same name (GND for example), name them like this: GND@1, GND@2, etc. They will show up in full in the Library editor, but the @ and everything after it will be invisible when the part is used in the schematic.
    e. Use 'text' to place '>NAME' and '>VALUE'
    f. Set Direction as follows:

        The Direction parameter specifies the logical direction of the signal flow:

        - NC Not connected
        - In Input
        - Out Output
        - I/O Input/output
        - OC Open Collector or Open Drain
        - Hiz High impedance output
        - Pas Passive (resistors, etc.)
        - Pwr Power pin (power supply input)
        - Sup Power supply output for ground and supply symbols

        The Electrical Rule Check executes, depending on the pin direction, various checks. It expects for the direction:

        - NC a not connected pin
        - In a net connected to this pin and not only *In* pins connected to this net

- Out not only *Out* pins connected to the net, no *Sup* or *OC* pin at the same net
- OC no *Out* pin at the same net
- Pwr a *Sup* pin set for this net
- I/O, Hiz, Pas no special checks

The *Pwr* and *Sup* directions are used for the automatic connection of supply voltages (see page 240).

3. Create device containing both package and schematic
4. Associate pins with pads in Connection dialog of Device window
5. Click on 'Description' below image of symbol to edit description for Library.
    a. (move up splitter from bottom if you don't see it)

6.2 Copying and moving devices

To copy a device from one library (source) to another (dest):

1. Open Control Panel, choose Dest library, OPEN it.
2. In Control Panel, find device you want and right click it. Choose 'Copy to Library.'
3. Repeat as desired (to same Dest library; Sources can differ).
4. Save updated library.

To rename or delete a device/package/symbol:

1. Open library that contains it.
2. Choose Library><Device/Package/Symbol>… (to load it)
3. Choose Library>Rename or Library>Delete
4. Save updated library.

To create a modified device from an existing device:

1. Open scratch library
2. Copy original part to scratch library
3. Rename part in scratch library
4. Open original library
5. Copy renamed part from scratch to original library
6. Modify part

Alternate method to copy an existing device for modification:

1. Open existing library symbol
2. Display all layers
3. Select everything with Group tool
4. Hit 'cut', then GO button (green traffic light) to copy everything into paste buffer (no ctrl keys)
5. Create new symbol
6. Give it a name
7. Paste in symbol (no ctrl keys)
8. Edit to taste

    a. Note – Eagle won't let you remove pins from Devices; you must work first on the Symbol and Package – 'remove' these from the Device first if necessary.
9. Repeat for package
10. Create new device, set value, name, pins

6.3 Supply symbols (special case)

Supply symbols (grounds, V+, etc.) are slightly different. They have a symbol but no package.

The pin is marked as type 'sup'.

Each different supply *must have its own unique symbol*, even if the symbol shape is identical (you can't reuse the same symbol for multiple voltages, even if in different Devices.)

The symbol pin Name *must* match the name of the signal that will be supplied ('GND', 'VBATT', etc.).

6.4 Pinswapping

Pins (or Gates) that have the same non-zero Swaplevel can be exchanged.

Swaplevel is defined in the Symbol (Pinswap) or Device (Gateswap)

Swaplevel 0 disables all swapping (use for polarized passives, for example).

If a non-polar passive (say, a resistor) has airwires that cross needlessly, probably the Swaplevel is set to 0. Instead of rotating it, try fixing it in the Library.

6.5 Updates

To update schematic or board after changes to library device/symbol/package use 'update'. To update all devices from all libraries in use, say 'update all'.

7 Board layout

7.1 Trace widths

Per IPC-2221 (from http://www.hardwarebook.info/PCB_trace), for 1 ounce copper (1 ounce/ft^2), in air, 1 inch trace length, 10 C acceptable rise, no special heat sinking, RMS average current:

Amps	*Outer layer Mils*	*Inner layer Mils*
0.010	0.1	0.3
0.050	0.6	1.5
0.100	1.2	3.1
0.200	2.3	6.2
0.400	4.7	12.3
0.500	5.9	15.4
0.600	7.1	18.5
0.700	8.3	21.5
0.800	9.5	24.6
0.900	10.6	27.7
1.0	11.8	30.8
1.5	20.7	53.8
2.0	30.8	80.0
2.5	41.9	109.0
3.0	53.8	140.0
4.0	80.0	208.0
5.0	109.0	283.0
6.0	140.0	364.0
7.0	173.0	451.0
8.0	208.0	542.0
9.0	245.0	637.0
10.0	283.0	737.0

Vias should be treated the same as 'inner layers' because, like them, they can't dissipate heat to the air. Assuming circumference = 2*Pi*r :

Via diameter (drill)	Equivalent trace width	Amps
13 mils	40.84 mils	~1.2
20 mils	62.83 mils	~1.6

7.2 Multilayer boards

For through vias no considerations about thickness of copper and isolation layers are necessary (see section above).

Join two layers by an asterisk (like 1*2 or 3*16) to one core and combine several cores. This is symbolized by a plus character (like in 1*2+3*4). The isolation layer between two copper layers is called prepreg.

To express the possibility to have vias through all layers the whole expression is set into parenthesis.

Setup Layer (in DRC dialog) – examples:

4 layers: (1*2+3*16)
6 layers: (1*2+3*4+5*16)
8 layers: (1*2+3*4+5*6+7*16)

Here vias always have the length 1 to 16. They are reachable from all layers.

7.3 Classes

Classes are used in board layout to specify things like trace width and isolation width. Typically, power classes are wider. You could have multiple power classes depending on current.

The default Class (0,0,0) takes its values from the design rules.

Other classes (power, high current, whatever) can take values that are allowed by the design rules, but cannot break those rules. The class 'width' is the minimum trace width.

7.4 Placing parts

Place parts on the board with regard to:

- Keeping interconnected devices nearby
- Liming run lengths and crossovers
- Minimizing trace capacitance when needed
- Minimizing EMI (antennas)

A general rule is that if you place SMD components so close that you have to fit them together like puzzle pieces, they are too close to route easily (at least on 2 layer boards with parts on both sides). Leave generous room around components for easy routing.

Use a placement grid of 0.05 millimeters. This is important to help with routing.

These layers must be active in the board view:

- 19 – Unrouted (without it you can't see airwires)
- 23 – tOrigins (can't move anything on top layer without this)
- 24 – bOrigins (can't move anything on bottom layer without this)

Use Smash to allow placement of part numbers, etc.

Lay out the board in the following order:

1. Clearly indicate board boundaries for fab house (where to cut)
2. Mounting holes and/or fiduciaries – use at least 3 per board to line up film layers.
3. I/O connectors, UI items like buttons and lights, other immovable objects.
4. Double check ALL mechanical interfaces & screw holes or you're *screwed.*
    a. Use t/bRestrict and t/bKeepout as necessary.
5. Components.

a. Think about thermal dissipation for hot components
b. Smash as needed to place silkscreen without overlap
c. Place decoupling caps first (trace length is critical)
d. Place other parts

8 Routing

8.1 Concepts

The settings in the DRC affect what the routers (both follow-me and automatic) will do – change these settings to affect the width and isolation of traces, etc.

'Clearance' sets the minimum isolation distance from other signals. 'Layer' chooses which layer copper will be drawn in (just where the cursor is for the Follow-Me router).

Ratsnest – redraws airwires via shortest path (after moving). Also fills in polygons.

Ripup – turns routes back into airwires:

- ripup; Ripup everything
- ripup ! GND VCC Ripup everything except given signals

Avoid 90 degree turns and 'T's – they can cause signal reflections. This especially important for high-speed signals (power matters less). Use 45 degree turns instead. Curves are even better, but may slow down autorouting.

8.2 Routing order

In general, it is not a good idea to use the autorouter for (1) thru (7) below; you want to control these items yourself by hand to make sure things go where they ought. For example, you want power and ground to reach the decoupling caps before the component; the autorouter doesn't know this.

So manually route (with the follow-me router, usually) items (1) thru (7) below before running the autorouter in step (9).

But to save time, before manually routing anything, run the autorouter on the original un-routed board just to see if it will complete (route 100% of the airwires). If it doesn't, you will have troubles routing the board as it is laid out. If that happens, look at where the autorouter had trouble and try to free up more space for traces in those areas, then try again.

Once you're confident the board can be routed as laid out, place traces in the following order:

1. Power & ground, using thick traces and a "star" configuration (parallel distribution, NOT serial). Very important for noise.
    a. Analog ground (if any); star configuration
    b. Hi-current power (> 500 mA)
    c. Hi-current ground
    d. Vdd (CMOS), or Vcc (TTL)
    e. Ground
2. High-frequency signals surrounded with pairs of ground traces.

3. For low altimeter noise, both VRef+ *and* power to pressure sensor must be EXACTLY common to each other and OUT OF THE PATH of radio & GPS (and other power-consumers). If you connect them in-line, Vdd variations will affect accuracy.
4. Decoupling capacitors (close)
5. Thermal dissipation copper (if needed)
6. Pin labels, etc. (Smash parts if needed to make things fit.)
7. Autoroute all other signals
8. Pours (ground planes, thermal, etc. - see below)
    a. Allow sufficient copper for heat sinking around LDO/vreg
    b. After pouring, ripup & re-route as needed to make pours work better, then re-pour
9. Manually fix anything autorouter can't do (use follow-me router)

Power and ground traces

Layout power and ground traces early. It is very important to avoid snaking or daisy chaining the power lines from part-to-part. Use a 'star' (parallel) distribution, not serial.

Try to use at least 10 mil for power and ground traces (even if low current).

Power and ground can be routed manually, but an automated way (if they are complex) is to do the following:

1. Layout *all* traces at nominal trace width (usually 8 mils).
2. Ripup the power traces one at a time, and re-autoroute them bigger. Start at the biggest width you want (typically 30 mils or so), then re-do with successively smaller widths until they're all routed. You may have to fix a few by hand. To do this:
    a. RIPUP small trace
    b. Set new width in DRC (controls autorouted width). Set via size too.
    c. Autoroute.
    d. Iterate (b) and (c) as needed.

High current traces

Use 8 mil traces for up to 500 mA, 20 mil traces for up to 1.5 A. For more, set DRC>Masks>Limit to 31 mils and use 31 mil drilled vias for 3A circuits.

High frequency signals

Surround with pairs of ground traces to help isolate EMI. Avoid "T" intersections.

8.3 Follow-me router

The follow-me router is most useful for manually routing things like decoupling caps and high-current traces (or entire boards). The autorouter can then be used to route (most of, usually) the remaining signals.

You MUST set the grid (standard, not alternate) to the grid you want the follow-me router to use. If the grid is not fine enough, the follow-me router will not route to some pins.

You can set the follow-me weights in the autorouter dialog (follow-me tab, then Select).

The Layer selection determines which layer the signal MUST be on at the cursor position.

You can force a via by switching layers.

8.4 Autorouter

The autorouter will use the *trace width and clearance specified in the DRC.*

The size of the 'grid' *in the autorouter dialog* (not the main 'grid') determines the *positioning* of autorouted nets. *0.05 mm is an excellent value*. (2 mils if using Imperial units).

The autorouter grid must be <= the placement grid, and should go *evenly* into the placement grid.

For TQFP 0.5mm pitch parts (PIC32MX4xx), the placement grid is 0.5mm (by definition; this is the pitch of the part), and the following parameters seemed to do a good job on a mixed thru-hole and SMD board (Rev4a):

- Routing grid 0.25 mm (placement grid/2)
- Top layer X direction
- Bottom layer Y direction (XY is slightly better than *. Didn't try *,X.)
- Via cost 5 (default)
- NonPref cost 8 (default was 1)

Routing fine-pitch components:

- Set a sufficiently fine autorouter grid
- Make sure the DRC minimum widths are small enough
- Make sure the DRC minimum clearances are small enough

But don't break the design rules of the PCB fab house.

General setup

- Set GROUND and POWER signals into a class that gives 10 to 16 mil traces before autorouting (wish I'd done this on Rev4a)
- If trace will carry more than ~ 1.6 A, use larger vias (31 mils vs standard 20 mil drills) for these signals (31 mils is enough for 3A). Set DRC>Masks>Limit to 31 mils to keep vias tented.
- Try to isolate high-current signals, setup appropriate classes for them
- Try to keep traces no smaller than 10 mil
- Try to keep isolation at 10 mil (move this to 8 mil before making the traces 8 mil)
- Try to leave 12 mil of isolation around a power plane pour
    - Double check ratsnest – this can break connections
- Vias
    - Tent vias (cover them with soldermask)
    - Use restrings ('rest-rings') of 12 mil or more (8 mil minimum)
- Silkscreen
    - Avoid silkscreen over bare copper – only on solderrmask
    - Mark board outline on the silkscreen

- Use only vector fonts

Board layout tips

In autorouter, select directions and weights for each layer.

If you have problems autorouting the board, try the following (in the given order):

1. Change isolation between signals from 10 mil to 8 mil (or 6 mil for 4-layer @ BatchPCB)
2. Change trace width from 10 mil to 8 mil (or 6 mil for 4-layer @ BatchPCB)
3. Change via restring size to 10, 8, or 6 mil (within design rules)
4. Change minimum drill to 13 mils (only for 4-layer @ BatchPCB)
5. For 4-layer boards, try setting the weights as follows:
    a. Bottom: 0
    b. Middle1: 10
    c. Middle2: 10 (or 'n/a' if used as a signal plane)
    d. Top: 50

8.5 Planes, pours and polygons

In Display Layers, rename layers to names of signal if you want a given layer to carry only one symbol. $ will be pre-pended to the name. (example: GND becomes $GND).

Note that polygon pours may not be needed if you have an internal ground plane.

You can use the 'polygon <signal>' command to draw a polygon that will get filled in ('pour') with a given signal. The polygon will avoid other signals by the given isolation distance.

Pour polygons *after* you have routed all signals.

Important – If you have overlapping pours (overlapping polygons), be aware that they are poured in rank order – Rank 0, then Rank 1, then ... Rank 7. Each pour *avoids* the pours previously poured. So the *inner* polygons must be poured *first*, so they must have the *lowest rank* (normally rank 1). Outer polygon should have higher ranks (so they are poured later).

An alternative to polygons is to simply draw Rectangle(s) of copper *before* routing – the autorouter will avoid areas that have already been routed, including your rectangle.

Don't forget to connect up the rectangle to a signal.

Activate signal planes with 'ratsnest' command (go from dotted outline of polygon to copper).

Deactivate signal planes with 'ripup' command (go from copper to dotted outline of polygon) – you must click outer edge of polygon (Eagle 'sees' only the outline).

To create ground and power planes with 'polygon'

1. Choose the 'polygon' tool.
2. Set the Width to the minimum trace width (8 mils for 2-sided BatchPCB) and the Isolate to the distance you want the plane isolated from other signals (minimum 8 mils for 2-sided BatchPCB).

3. Draw the outlines of the area where you want the plane. Draw in the same layer where you want the plane copper.
4. Use the 'name' command to name the polygon the same name as the signal you want it to carry.
    a. Change name of the Polygon – 'ratsnest' will connect the plane to the signal with new name
    b. Change name of 'entire Signal' – if name matches an existing signal, you will get a confirmation dialog to see if you want them connected
5. Hit 'ratsnest' to fill in the copper.

Note that 'spacing' only matters when doing hatched (not solid) polygons.

To pour effective HEATSINK copper

Pour a small area 'solid, *without* thermals' areas copper around the device pins, to get the heat out of the pin and into the copper. Use a small width (10 mil or so).

Pour 'solid WITH thermals' over a larger area to spread out the heat. This will leave the surrounded components still easily solderable. Use a large width (30 mils or so).

Improving pours

After you pour copper, especially over a large area, you can manually move traces and vias around so that the pour will reach otherwise-orphaned areas.

This can be done by a combination of:

- Moving traces and vias with the Move tool. Once you've moved things, re-run the DRC to check for problems. To clean up angles, etc., you can rip-up misplaced traces and let the autorouter replace them with neat 90 and 45-degree angle traces.
- Ripping up the signals, placing temporary 'restrict' areas, and re-running the autorouter to place new traces avoiding the restricted areas.

9 Generating gerber files

9.1 2-layer boards

1. Open the board.
2. Select ALL layers to display
3. File>CAM Processor>File>Open>Job...
4. Choose 'Dave-gerb274x(2layer).cam'. The layers output have been modified from Sparkfun's version.
5. Click OPEN
6. Click PROCESS JOB.

Output files will go into the project folder.

Check the output files using Viewplot or similar before transmission.

It should produce exactly 7 files that you need to zip and send to the fab house:

- Top and bottom copper (.GTL, .GBL)
- Top and bottom solder mask (.GTS, .GBS)
- Top and bottom silkscreen (.GTO, .GBO)
- Drill file, 2.4 leading (.TXT)

It will also produce 2 files that you don't need to send:

- .GTP (top paste)
- .gpi (general board info)

Put the 7 files above into a .ZIP file and upload to BatchPCB.com.

9.2 4-layer boards

Activate ALL layers.

Use '4LayerBatchPCBGerbers.cam'. The layers output have been modified from Sparkfun's version and Sunstone's (PCBExpress) files.

Check the output files using Viewplot or similar before transmission.

It should produce exactly 9 files that you need to zip and send to the fab house:

- Top and bottom copper (.GTL, .GBL)
- Mid-layers 1 and 2 (.G2, .G3)
- Top and bottom solder mask (.GTS, .GBS)
- Top and bottom silkscreen (.GTO, .GBO)
- Drill file, 2.4 leading (.TXT)

(Note that the one time I've tried this so far I got unusable boards...)

10 Assembly tips

- Diode polarity (LEDs too)
    - Marking is on cathode (usually a line, dot, or broken bar)

- Capacitor polarity (for polar caps)
    - On tantalum caps, bar marks the + (anode) side.
    - On electrolytic caps, the – (cathode) side is usually marked

11 Files and settings

11.1 User-language programs (ULPs)

To get a parts list (BOM), use 'bom.ulp'

11.2 Default trace widths

Set default trace widths in eagle.scr:

```
Set WIRE_BEND 1; #Route with 45 degree angles
Set Drill 0.02; #Make vias 0.02"
Change Shape Round; #Make vias round
Change Width 0.01; #Routing width default to 10mil
```

11.3 Default DRU file

The default eagle DRU file is used, with the following modifications recommended by SparkFun (note # comments are not parsable):

```
mdCopperDimension = 10mil
      # Copper signal isolation minimum distance.  Eagle default 40mil.
msWidth = 8mil
      # Copper trace min width.  Eagle default 10mil.
msDrill = 20mil
      # Minimum drill diameter.  Eagle default 24 mil.
rlMinPadTop = 12mil
      # Min top rest ring diameter.  Eagle default 10 mil.
rlMinPadBottom = 12mil
      # Min bottom rest ring diameter.  Eagle default 10 mil.
rlMinViaOuter = 10mil
      # Min via diameter.  Eagle default 8 mil.
rlMinViaInner = 10mil
      # Min via diameter.  Eagle default 8 mil.
mlViaStopLimit = 25mil
      # minimum via stop mask diameter. Forces tented vias. Def=0mil.
```

Note that a 'restring' (rest ring) is the ring around the via visible on the outer layers of the board.

11.4 EAGLE.SCR

Eagle loads *eagle.scr* upon startup. This defines many settings and defaults.

That is the ONLY script that loads automatically.

Other ways to load/run scripts:

Command line: '–S filename'
Command 'script <filename>'.

11.5 .PRO files

.PRO files are stored in the project folder. They are Eagle's log of the autorouter's result, in plain ASCII. They are safe to delete.

Appendix A – Autopilot PCB Notes

- Mount USB on side or vertically (access easily once mounted)
- Mount pressure sensor
    - On bottom of board (keep away from sunlight)
    - PRESSURE signal with GND on either side for shielding, and close to PIC input

[end]