

32768 Bit Serial Read Only Memory

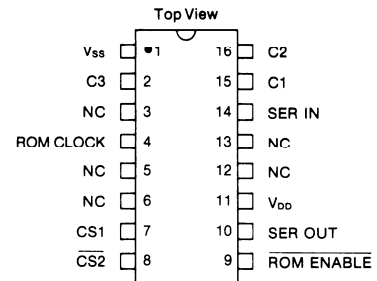
FEATURES

- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Tri-State Outputs
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

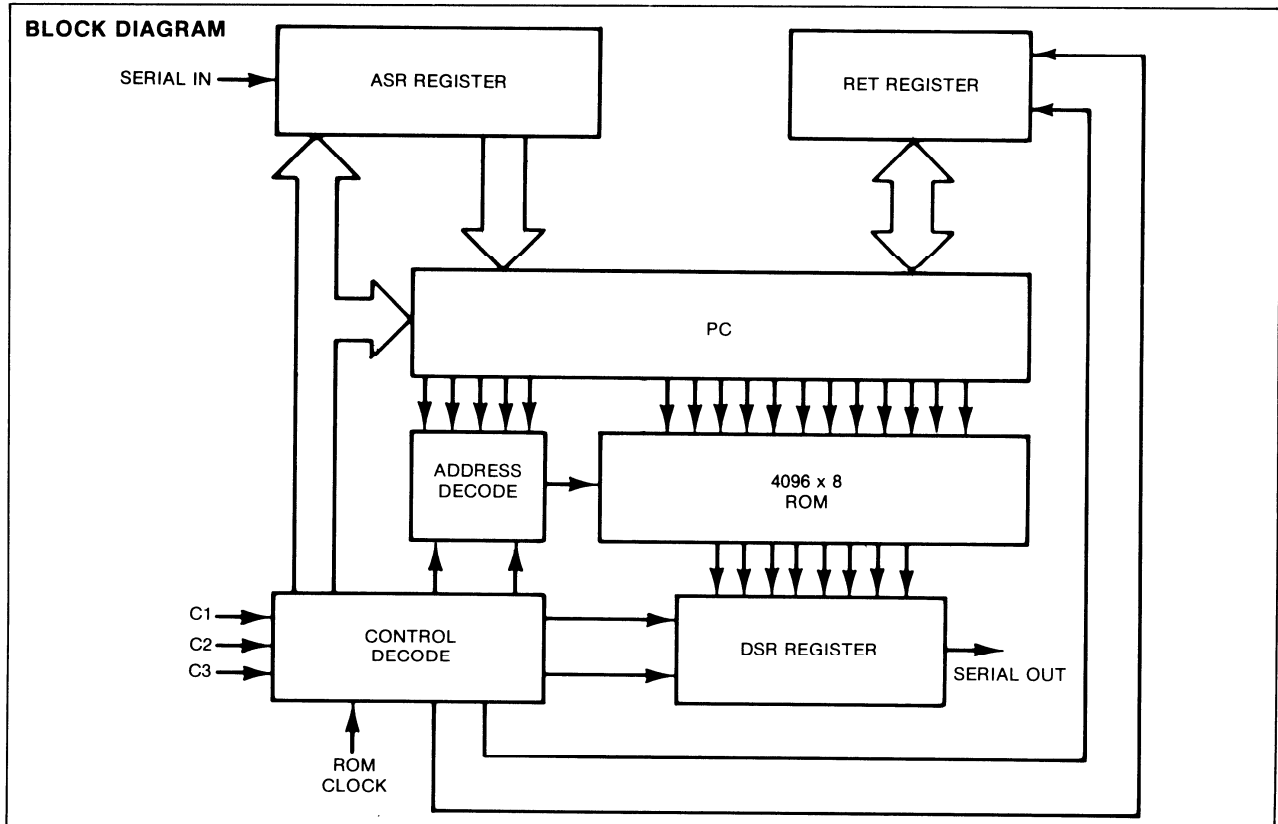
DESCRIPTION

The General Instrument SPR-32 is a 32,768 Bit Serial Read Only Memory organized as 4096 eight-bit words and is ideally suited for interfacing with the SP-0256 Speech Processor. Fabricated in General Instrument's advanced N-Channel Ion-Implant process to enable operation from a single +5 Volt power supply, up to 10 SPR-32s can be interfaced to the SP-0256 without buffering.

PIN CONFIGURATION 16 PIN DUAL IN LINE



BLOCK DIAGRAM



PIN ASSIGNMENTS (PRELIMINARY)

Pin Number	Name	Function
9	ROM ENABLE	Active low chip select used in system to eliminate bus conflict at system start-up. When brought high, ROM Enable Tri-States Serial Out (Pin 3).
14	SERIAL IN	Serial Input used to load 16 bit address into device.
10	SERIAL OUT	Output pin used to shift out data byte.
7	CS1	Active high chip select. Will Tri-State Serial output when low.
8	CS2	Active low chip select. Will Tri-State Serial output when high.
4	ROM CLOCK	1.56MHz clock input from SP-0256 speech processor.
1	V _{SS}	Ground pin.
2	C3	Control pins decoded to determine device function.
16	C2	
15	C1	
11	V _{DD}	Positive supply pin (+4.6V to +7.0V).

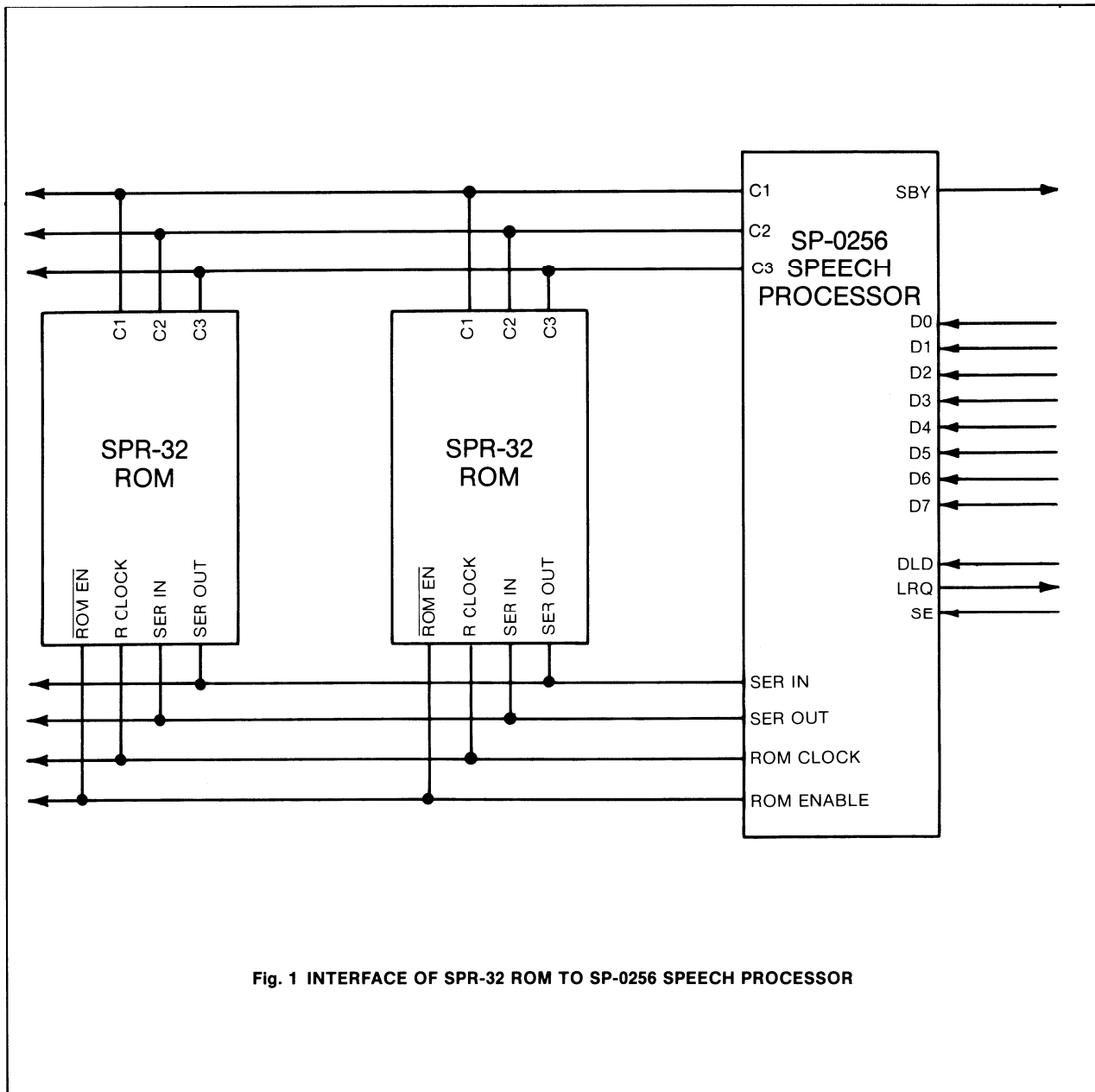


Fig. 1 INTERFACE OF SPR-32 ROM TO SP-0256 SPEECH PROCESSOR

TABLE 1 SPR-32 CONTROL STATES

C1	C2	C3	FUNCTION	
0	0	0	NOP	No action taken.
0	0	1	ASR Load	Accepts data from the serial input, synchronous to the externally supplied ROM clock. This data is shifted into the ASR holding register in preparation for loading into the PC. Although ASR is 16 bits long, it is not necessary to load all 16 bits of address sequentially in one ASR load.
0	1	0	PC Load	Loads the contents of the ASR register into the PC.
0	1	1	DSR Load	Loads the 8 bits of data pointed to by the present value of the least significant 11 bits of the PC into the data output shift register (DSR). At the completion of the DSR load the PC is incremented.
1	0	0	DSR Shift Out	Shifts out the contents of DSR to the serial out pin, synchronous to the ROM clock.
1	0	1	RET. Register Load	Loads the return register (RET) with the current value of the P.C.
1	1	0	Return	Loads the PC with the contents of the RET register.
1	1	1	NOP	No action taken.

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{DD} -3 to +12V
 Storage Temperature -25° to +125° C
 Lead Temperature (soldering) 10 Sec +333° C

Standard Conditions (unless otherwise stated)

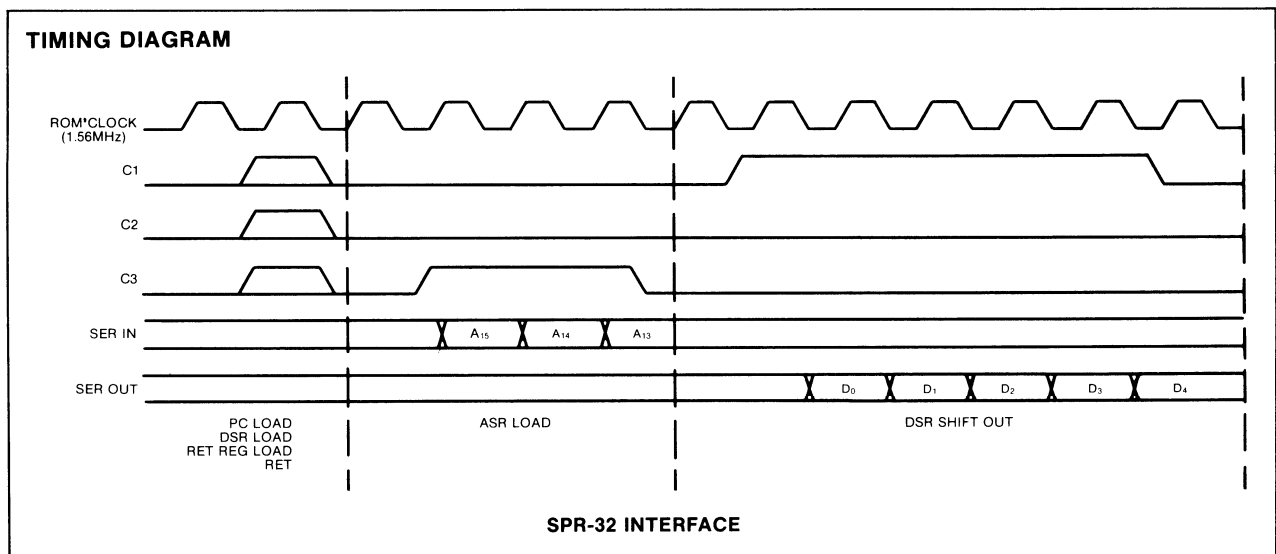
V_{DD} = +4.6V to +7.0V
 Operating Temperature = 0° C to +55° C

Supply Current

I_{DD} 25mA V_{DD} = 7.0V ROM clock frequency typically 1.56MHz
 V_{SS} = 0.0V

DC CHARACTERISTICS

Characteristic	Min	Max	Units	Conditions
Inputs				
ROM ENABLE, SERIAL IN, CS1, CS2, C1, C2, C3				
ROM Clock				
Logic 0	0.0	.4	V	
Logic 1	2.2	V _{DD}	V	
Capacitance		10	pF	
Leakage		10	μA	
Outputs				
SERIAL OUT				
Logic 0	0.0	.6	V	1.6mA
Logic 1	2.4	V _{DD}	V	50μA



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