



# TECHNICAL DATA

AN EXCLUSIVE RADIO SHACK SERVICE TO THE EXPERIMENTER

## SP0256-AL2 Voice Synthesizer

### Features

- Natural Speech
- Stand Alone Operation with Inexpensive Support Components
- Wide Operating Voltage
- Word, Phrase, or Sentence Library, ROM Expandable
- Expandable to 491K of ROM Directly
- Simple Interface to Most Microcomputers or Microprocessors
- Supports L.P.C. Synthesis: Formant Synthesis: Allophone Synthesis

### Description

The SP0256 (Speech Processor) is a single chip N-Channel MOS LSI device that is able, using its stored program, to synthesize speech or complex sounds.

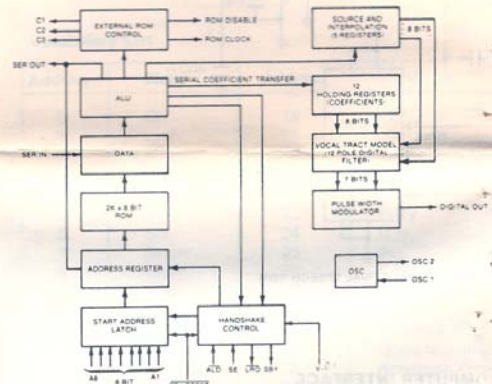
The achievable output is equivalent to a flat frequency response ranging from 0 to 5kHz, a dynamic range of 42dB, and a signal-to-noise ratio of approximately 35dB.

The SP0256 incorporates four basic functions:

- A software programmable digital filter that can be made to model a VOCAL TRACT.
- A 16K ROM which stores both data and instructions (THE PROGRAM).
- A MICROCONTROLLER which controls the data flow from the ROM to the digital filter, the assembly of the "word strings" necessary for linking speech elements together, and the amplitude and pitch information to excite the digital filter.
- A PULSE WIDTH MODULATOR that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

### Applications

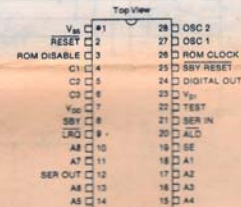
- Telecommunications
- Appliances
- Computer Peripherals
- Automotive
- Personal Computers
- Toys/Games
- Educational Aids
- Warning Systems
- Security Systems
- Electronic Musical Instruments
- Aids to the Blind
- Narrow Bandwidth
- Communication Systems



BLOCK DIAGRAM FOR SP0256

### PIN CONFIGURATION

28 LEAD DUAL IN LINE



### Absolute Maximum Ratings

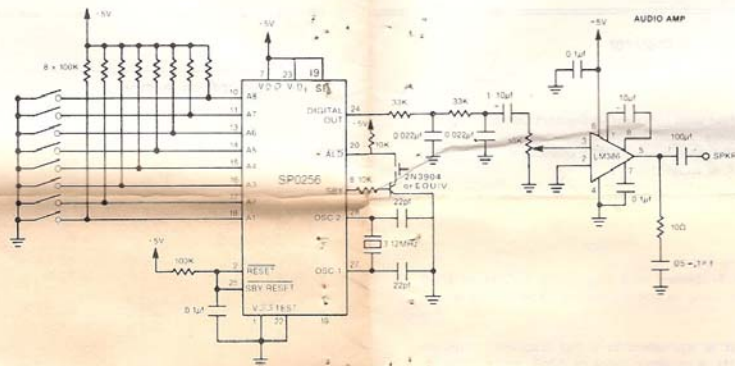
V <sub>D1</sub> V <sub>DD</sub>	-0.3V to +12V
Storage Temperature	-25°C to +125°C
Clock Crystal Frequency	3.12MHz

### DC CHARACTERISTICS

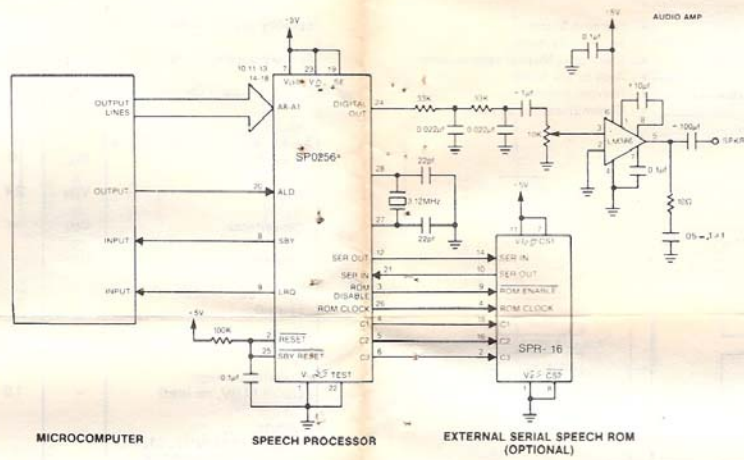
Operating Temperature T<sub>A</sub> = 0°C to +70°C

Characteristics	Sym	Min	Max	Units
Primary Supply Voltage	V <sub>DD</sub>	4.6	7	V
Standby Supply Voltage	V <sub>D1</sub>	4.6	7	V
Primary Supply Current	I <sub>DD</sub>	-	90	mA
Standby Supply Current	I <sub>D1</sub>	-	-	mA
<b>Inputs</b>				
A1-A8, ALD, SER IN, TEST, SE Logic 0	V <sub>IL</sub>	0	0.6	V
Logic 1	V <sub>IH</sub>	2.4	V <sub>D1</sub>	V
Capacitance	C <sub>IN</sub>	-	10	pf
Leakage	I <sub>LC</sub>	-	± 10	μA
<b>RESET, SBY RESET</b>				
Logic 0	V <sub>IL1</sub>	0	0.6	V
Logic 1	V <sub>IH1</sub>	3.6	V <sub>D1</sub>	V
<b>Oscillator Leakage</b>				
OSC 1 (7.0V, no load)	-	1.0	10	μA
<b>Outputs</b>				
SBY, DIGITAL OUT, C1, C2, C3, LRO, ROM DISABLE, ROM CLOCK, SER OUT Logic 0 (0.72mA load)	V <sub>OL</sub>	0	0.6	V
Logic 1 (-50μA load)	V <sub>OH</sub>	3.5	V <sub>D1</sub>	V

CUSTOM PACKAGED IN USA BY RADIO SHACK, A DIVISION OF TANDY CORPORATION



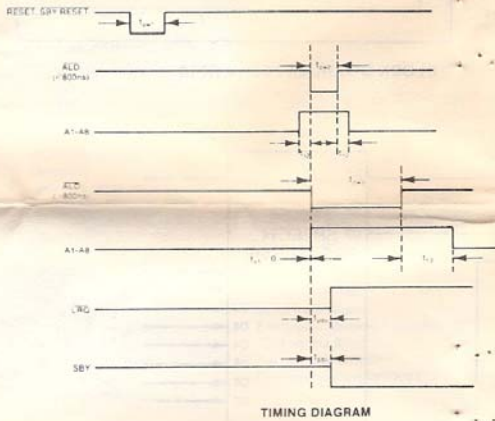
TYPICAL APPLICATION STAND ALONE CONFIGURATION



TYPICAL APPLICATION MICROCOMPUTER INTERFACE

**AC CHARACTERISTICS**  
Operating Temperature:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$

Characteristics	Sym	Min	Max	Units
Clock Frequency, 3.120 MHz	—	—	—	MHz
Reset, $\overline{\text{SBY}}$ Reset	$t_{pw1}$	100	—	$\mu\text{s}$
$\overline{\text{ALD}} (< 800\text{ns})$	$t_{pw2}$	200	800	ns
A1-A8 Set Up	$t_{s2}$	160	—	ns
A1-A8 Hold	$t_{h2}$	160	—	ns
$\overline{\text{ALD}} (\geq 800\text{ns})$	$t_{pw3}$	800	—	ns
A1-A8 Set Up	$t_{s3}$	0	—	ns
A1-A8 Hold	$t_{h3}$	1200	—	ns
$\overline{\text{LRQ}}$	$t_{pd0}$	—	640	ns
$\overline{\text{SBY}}$	$t_{pd0}$	—	640	ns



TIMING DIAGRAM

**Vocabulary List**

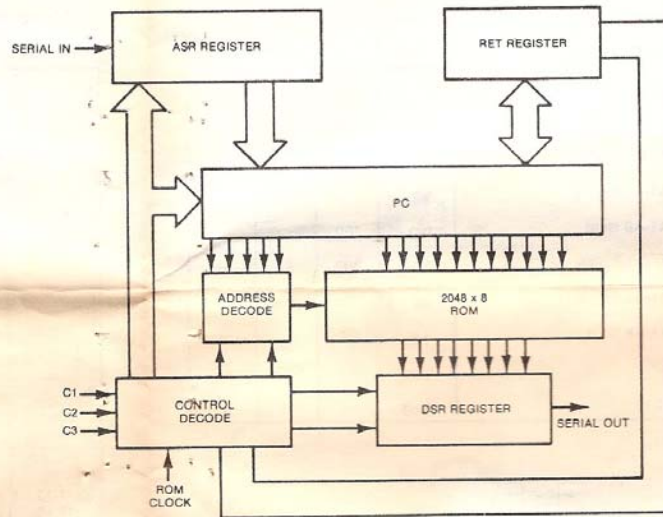
Address	Word	Address	Word
0	Oh	18	Eighteen
1	One	19	Nineteen
2	Two	20	Twenty
3	Three	21	Thirty
4	Four	22	Forty
5	Five	23	Fifty
6	Six	24	It Is
7	Seven	25	A.M.
8	Eight	26	P.M.
9	Nine	27	Hour
10	Ten	28	Minute
11	Eleven	29	Hundred Hour
12	Twelve	30	Good Morning
13	Thirteen	31	Attention Please
14	Fourteen	32	Please Hurry
15	Fifteen	33	Melody A
16	Sixteen	34	Melody B
17	Seventeen	35	Melody C

**PIN FUNCTIONS**

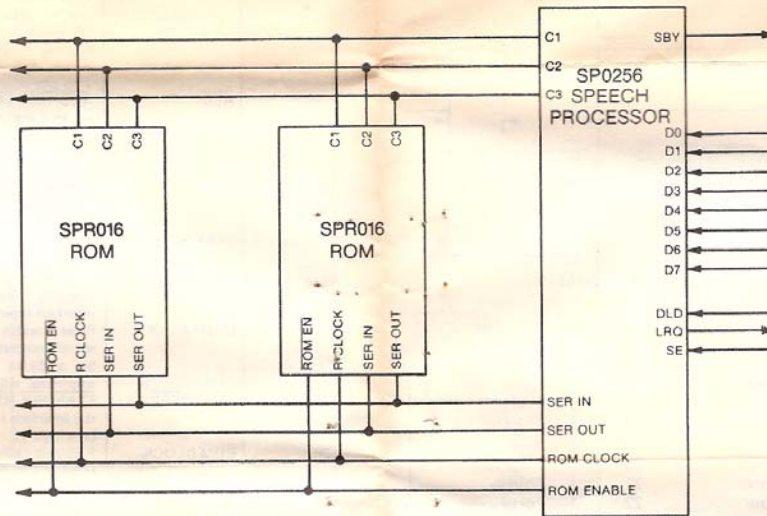
Pin Number	Name	Function
1	$V_{SS}$	Ground
2	$\overline{\text{RESET}}$	A logic 0 resets the SP. Must be returned to a logic 1 for normal operation.
3	ROM DISABLE	For use with an external serial speech ROM. A logic 1 disables the external ROM.
4,5,6	C1,C2,C3	Output control lines used by an external serial speech ROM.
7	$V_{DD}$	Primary power supply.
8	$\overline{\text{SBY}}$	STANDBY. A logic 1 output indicates that the SP is inactive (i.e. not talking) and $V_{DD}$ can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, $\overline{\text{SBY}}$ will go to logic 0.
9	$\overline{\text{LRQ}}$	LOAD REQUEST. $\overline{\text{LRQ}}$ is a logic 1 output whenever the input buffer is full. When $\overline{\text{LRQ}}$ goes to a logic 0, the input port is loaded by placing the 8 address bits on A1-A8 and pulsing the $\overline{\text{ALD}}$ input.
10,11,13,14,15,16,17,18	A8,A7,A6,A5,A4,A3,A2,A1	8-bit address which defines any one of 256 speech entry points.
12	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM.
19	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, $\overline{\text{ALD}}$ is disabled and the SP will automatically latch in the address on the input bus approximately $1\mu\text{s}$ after detecting a logic 1 on any address line.
20	$\overline{\text{ALD}}$	ADDRESS LOAD. A negative pulse on this input loads the 8 address bits into the input port. The leading edge of this pulse causes $\overline{\text{LRQ}}$ to go high.
21	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22	TEST	A logic 1 places the SP in test mode. This pin should normally be grounded.
23	$V_{D1}$	Standby power supply for the interface logic and controller.
24	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5kHz low pass filter and amplified, will drive a loudspeaker.
25	$\overline{\text{SBY}}$ RESET	STANDBY RESET. A logic 0 resets the interface logic. Normally should be a logic 1.
26	ROM CLOCK	1.56MHz clock for an external serial speech ROM.
27	OSC 1	XTAL IN. Input connection for a 3.12MHz crystal.
28	OSC 2	XTAL OUT. Output connection for a 3.12MHz crystal.



Pin Configuration for SPR016



BLOCK DIAGRAM FOR SPR016



Simple Interface of SPR016s to SP0256

RADIO SHACK, A DIVISION OF TANDY CORPORATION

U.S.A.: FORT WORTH, TEXAS 76102  
CANADA: BARRIE, ONTARIO L4M 4W5

TANDY CORPORATION

AUSTRALIA	BELGIUM	U. K.
91 KURRAJONG ROAD MOUNT DRUITT, N.S.W. 2770	PARC INDUSTRIEL DE NANINNE 5140 NANINNE	BILSTON ROAD WEDNESBURY WEST MIDLANDS WS10 7JN