



# AY38910A AY38912A

## PROGRAMMABLE SOUND GENERATOR

### FEATURES

- Industry standard programmable sound generator
- Register oriented architecture for ease of use
- Full software control of sound generation
- Easily interfaces to most 8-bit and 16-bit microprocessors
- Three independently programmable analog outputs
- One or two 8-bit I/O ports
- Single 5 volt supply
- 0° to 70° C operation
- 40 pin or 28 pin package option

### APPLICATIONS

- Arcade games
- Warning alarms
- Special effects
- Personal computers
- Music synthesis

### DESCRIPTION

The AY38910A/38912A Programmable Sound Generator (PSG) is an LSI circuit which can produce a wide variety of complex sounds under software control. The AY38910A/38912A is manufactured in Microchip Technology's N-Channel Ion Implant Process. Operation requires a single +5V power supply, a compatible clock, and a microprocessor controller, such as the PIC series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signaling, and personal computer usage. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one component is satisfied by the three independently controllable analog sound output channels can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

### PIN CONFIGURATION Top View

#### 40 LEAD DUAL INLINE - AY38910A

Vss (GND)	1	40	Vcc (+5V)
No Connect	2	39	No Connect
Analog Channel B	3	38	Analog Channel C
Analog Channel A	4	37	DA0
No Connect	5	36	DA1
IOB7	6	35	DA2
IOB6	7	34	DA3
IOB5	8	33	DA4
IOB4	9	32	DA5
IOB3	10	31	DA6
IOB2	11	30	DA7
IOB1	12	29	BC1
IOB0	13	28	BC2
IOA7	14	27	BDIR
IOA6	15	26	No Connect
IOA5	16	25	A8
IOA4	17	24	A9
IOA3	18	23	RESET
IOA2	19	22	Clock
IOA1	20	21	IOA0

#### 28 LEAD DUAL INLINE - AY38912A

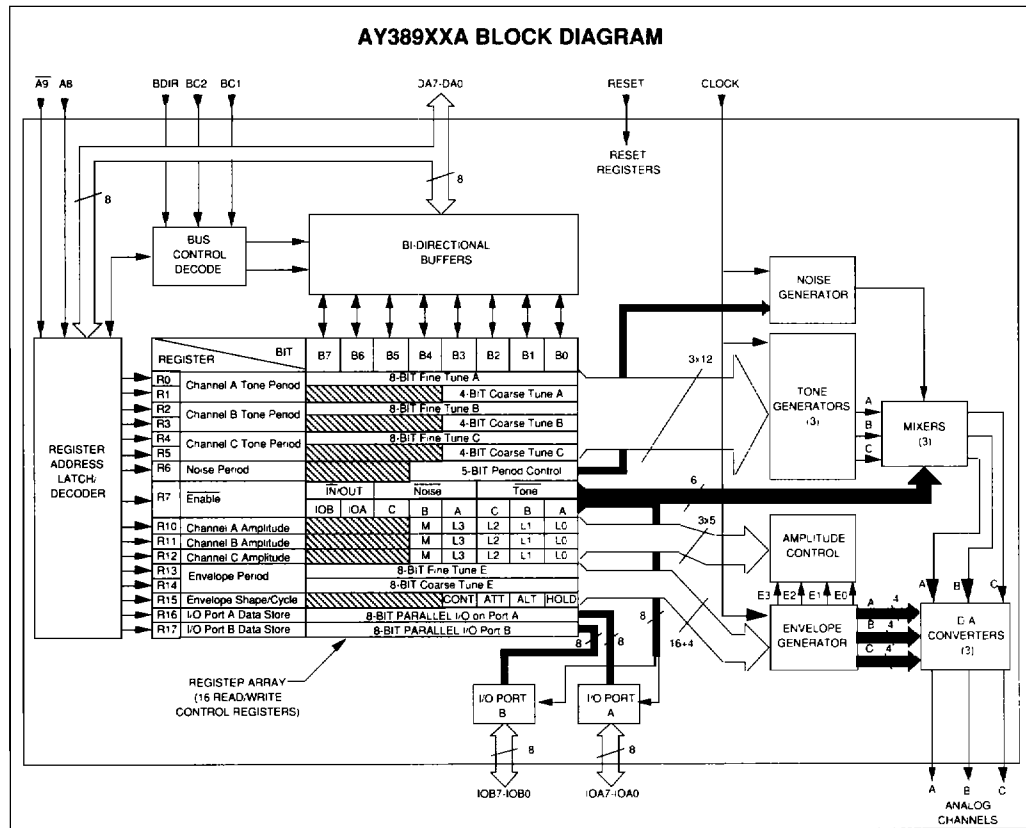
Analog Channel C	1	28	DA0
No Connect	2	27	DA1
Vcc (+5V)	3	26	DA2
Analog Channel B	4	25	DA3
Analog Channel A	5	24	DA4
Vss (GND)	6	23	DA5
IOA7	7	22	DA6
IOA6	8	21	DA7
IOA5	9	20	BC1
IOA4	10	19	BC2
IOA3	11	18	BDIR
IOA2	12	17	A8
IOA1	13	16	RESET
IOA0	14	15	Clock

# AY38910A/AY38912A

## DESCRIPTION (CTD.)

All circuit control signals are digital in nature and may be provided directly by a microprocessor/microcomputer. Therefore, one PSG can produce the full range of required sounds with no change in external

circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction.



## PIN FUNCTIONS

### DA7-DA0 (Input/Output/High Impedance)

Data/Address Bits 7-0: Pins 30-37 (AY38910A)  
Pins 21-28 (AY38912A)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the address mode, DA3-DA0 select the internal register address (0-17<sub>8</sub>) and DA7-DA4 in conjunction with address inputs A9 and A8, form the chip select function. When the high order address bits are "incorrect", the bidirectional buffers are forced to a high impedance state.

### Address 9, Address 8

A8 (input): Pin 25 (AY38910A)  
Pin 17 (AY38912A)  
A9 (input): Pin 24 (AY38910A)  
Not available (AY38912A)

High order address bits A9 and A8 are fixed to recognize a "01" code. They may be left unconnected as each is provided with either an on chip pull-down (A9) or pull-up (A8) resistor. In noisy environments, however, it is recommended that A9 and A8 be tied to external ground and +5V respectively if they are not to be used.

## RESET (Input)

Pin 23 (AY38910A)  
Pin 16 (AY38912A)

For initialization/power-on purposes, applying a low level input to the RESET pin will reset all registers to 0<sub>8</sub>. The RESET pin is provided with an on-chip pull-up resistor.

## CLOCK (Input)

Pin 22 (AY38910A)  
Pin 15 (AY38912A)

This TTL compatible input supplies the timing reference for the Tone, Noise, and Envelope Generators.

## BDIR, BC2, BC1 (Inputs)

Pins 27,28,29 (AY38910A)  
Pins 18,19,20 (AY38912A)

The Bus DIRection, Bus Control 2 and Bus Control 1 are

used to control the PSG.

For example, if these bus control signals are generated directly by a microprocessor to control all bus operations internal and external to the PSG, then the following Bus Control Function Table applies.

Interfacing to a processor simply requires simulating the decoding shown in the Function Table. The redundancies in the PSG functions vs. bus control signals can be used as an advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could reduce the programming of the bus control signals to the following Simplified Bus Control Function Table which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V).

BUS CONTROL FUNCTION TABLE				
BDIR	Inputs BC2	BC1	Microprocessor Function	PSG Function
0	0	0	NACT	INACTIVE. See 010 (IAB) below.
0	0	1	ADAR	LATCH ADDRESS. See 111 (INTAK) below.
0	1	0	IAB	INACTIVE. The PSG/CPU bus is inactive. DA7-DA0 are in a high impedance state.
0	1	1	DTB	READ FROM PSG. This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7-DA0 are in the output mode.
1	0	0	BAR	LATCH ADDRESS. See 111 (INTAK) below.
1	0	1	DW	INACTIVE. See 010 (IAB) above.
1	1	0	DWS	WRITE TO PSG. This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7-DA0 are in the input mode.
1	1	1	INTAK	LATCH ADDRESS. This signal indicates that the bus contains a register address which should be latched in the PSG. DA7-DA0 are in the input mode.

SIMPLIFIED BUS CONTROL FUNCTION TABLE				
BDIR	Inputs BC2	BC1	PSG Function	
0	1	0	INACTIVE.	
0	1	1	READ FROM PSG.	
1	1	0	WRITE TO PSG.	
1	1	1	LATCH ADDRESS.	

# AY38910A/AY38912A

## Analog Channel A, B, C (Outputs)

Pins 4,3,38 (AY38910A)

Pins 5,4,1 (AY38912A)

Each of these signals is the output of its corresponding digital to analog converter and provides 1V peak-peak (max) signal representing the complex sound wave-shape generated by the PSG.

## No Connect

Pins 2,5,26,39 (AY38910A)

Pin 2 (AY38912A)

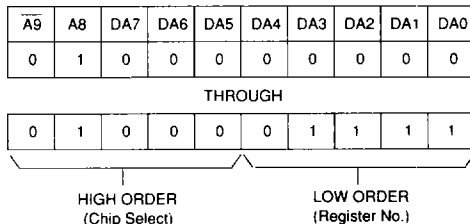
These pins are for Microchip Technology test purposes

## ARCHITECTURE

The AY38910A/AY38912A is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values. All functions of the PSG are controlled through the 16 registers which, once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

## Register Array

The principle element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and as such occupy a 16 word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits) are decoded as follows:



The four low order address bits select one of the 16 registers (R0a-R17a). The six high order address bits function as chip selects to control the tri-state bidirectional buffers (when the high order address bits are incorrect, the bidirectional buffers are forced to a high impedance state). High order address bits A9, A8 are fixed in the PSG design to recognize a "01" code; high order address bits DA7-DA4 are programmed to recognize only a "0000" code. All addresses are latched internally. This internally latched address is updated

only and should be left open. Do not use as tie-points.

## Vcc

Pins 40 (AY38910A)

Pin 3 (AY38912A)

Nominal +5 Volt power supply to the PSG.

## Vss

Pin 1 (AY38910A)

Pin 6 (AY38912A)

Ground reference for the PSG.

and modified on every latch address signal presented to the PSG via the BDIR, BC2 and BC1 inputs. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (Inactive, Latch Address, Write Data) is accomplished by the Bus Control Decode block.

## Sound Generating Blocks

The basic blocks in the PSG which produce the programmed sounds include:

- Tone Generators**      Produce the basic square wave tone frequencies for each channel (A, B, C).
- Noise Generator**      Produces a pulse width modulated pseudo-random square wave output.
- Mixers**      Combine the outputs of the Tone Generators and the Noise Generator; per channel (A,B,C).
- Envelope Generator**      Produces an envelope pattern which can be used to amplitude modulate the output of each Mixer.
- Amplitude Control**      Provides the D/A Converters with either a fixed or variable amplitude pattern. Fixed amplitude is under direct CPU control. Variable amplitude is accomplished via the output of the Envelope Generator.
- D/A Converters**      The three D/A Converters each produce a 16 level (max) output signal as determined by the Amplitude Control.

## OPERATION

Since all PSG functions are processor controlled by writing to the internal registers (see table). A detailed description of the PSG operation may best be accomplished by relating each PSG function to control of the corresponding register. The function of creating or programming a specific sound effect logically follows the control sequence shown in the figure below.

### Tone Generator Control (R0 - R5)

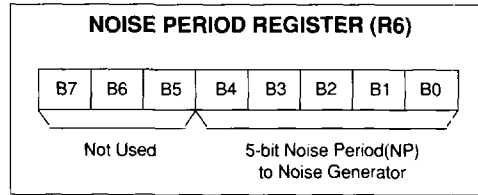
The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained by first dividing the input clock by 16 then by further dividing the result by the programmed 12 bit Tone Period value. Each 12-bit tone period value is obtained by combining the contents of the respective Coarse and Fine Tune registers, as illustrated.

INTERNAL REGISTERS		
Operation	Register	Function
Tone Generator Control	R0-R5	Program tone periods
Noise Generator Control	R6	Program noise period
Mixer Control	R7	Enable tone and/or noise on selected channels
Amplitude Control	R10 <sub>8</sub> -R12 <sub>8</sub>	Select fixed or variable (envelope) amplitudes
Envelope Generator Control	R13 <sub>8</sub> -R15 <sub>8</sub>	Program envelope period, select envelope pattern

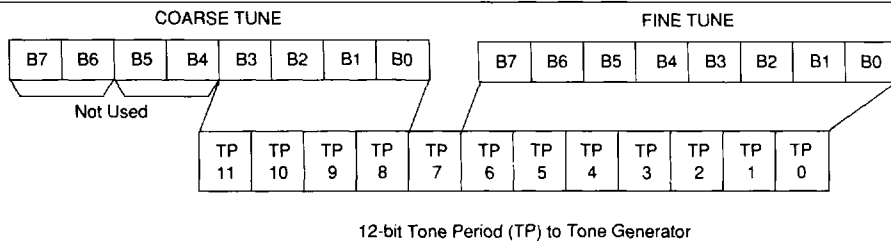
TUNE REGISTERS		
Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2

### Noise Generator Control ( R6)

The frequency of the noise source is obtained by dividing the input clock by 16, then by further dividing the result by the programmed 5 bit Noise Period value. This 5 bit value consists of the lower 5 bits (B4-B0) of register R6, as illustrated:



## CONTROL SEQUENCE



- Notes:**
- The period of the output of the tone generator is therefore determined by:  $16 \times TP \times P$  where  $P =$  the period of the input clock.
  - If the Coarse and Fine Tune registers are both set to 0008, the resulting period will be minimum, i.e., the generated tone period will be as if the Coarse Tune register was set to 0008 and the Fine Tune register set to 0018.

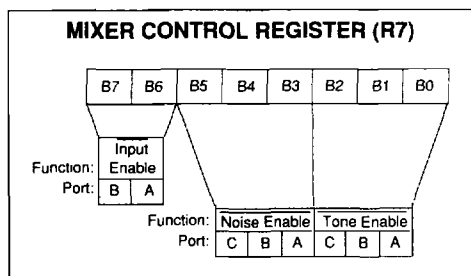
# AY38910A/AY38912A

## Mixer Control - I/O Enable (R7)

Register R7 is a multi-function **ENABLE** register which controls the three Noise/Tone Mixers.

The mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5-B0 of register R7, as illustrated.

The direction (input or output) of the general purpose I/O ports (I/OA and I/OB) is determined by the state of bits B7 and B6 of R7, as illustrated.



**NOISE ENABLE TRUTH TABLE**

R7 Bits B5 B4 B2	Noise Enabled on Channel
0 0 0	C B A
0 0 1	C B -
0 1 0	C - A
0 1 1	C - -
1 0 0	- B A
1 0 1	- B -
1 1 0	- - A
1 1 1	- - -

**TONE ENABLE TRUTH TABLE**

R7 Bits B2 B1 B0	Tone Enabled on Channel
0 0 0	C B A
0 0 1	C B -
0 1 0	C - A
0 1 1	C - -
1 0 0	- B A
1 0 1	- B -
1 1 0	- - A
1 1 1	- - -

**I/O PORT TRUTH TABLE**

R7 bits B7 B6	I/O Port Status I/OB I/OA
0 0	Input Input
0 1	Input Output
1 0	Output Input
1 1	Output Output

NOTE: Disabling noise and tone does not turn off a channel. Turning a channel off can only be accomplished by writing all zeros into the corresponding Amplitude Control Register.

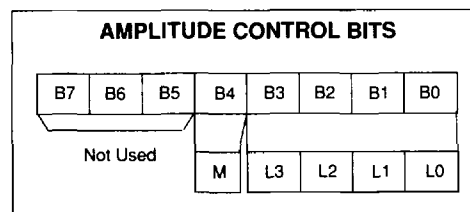
## Amplitude Control (R10<sub>a</sub>, R11<sub>a</sub>, R12<sub>a</sub>)

The amplitude of the signals generated by each of the three D/A Converters (one each for Channels A, B, and C) is determined by the content of the lower bits (B4-B0) of registers R10<sub>a</sub>, R11<sub>a</sub>, and R12<sub>a</sub> as illustrated.

These five bits consist of a 1-bit mode select ("M" bit) and a 4-bit "fixed" amplitude level (L3-L0). When the M bit is low, the output level of the analog channel is defined by the 4-bit "fixed" amplitude level of the Amplitude Control Register. This amplitude level is fixed in the sense that the amplitude

**CHANNEL CONTROL**

Register	Channel
R10 <sub>a</sub>	A
R11 <sub>a</sub>	B
R12 <sub>a</sub>	C



**AMPLITUDE CONTROL REGISTER**

Amplitude Mode	4 bit fixed Amplitude Level	Note
0	0 0 0 0	Amplitude Defined By L0-L3
.	.	
.	.	
.	.	
0	1 1 1 1	Amplitude Defined
1	X X X X	

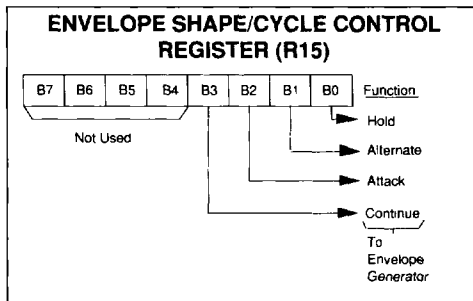
is under direct control of the system processor. When the M bit is high, the output level of the analog channel is defined by the 4-bits of the Envelope Generator (bits E3-E0). The amplitude mode bit can also be thought of as an "envelope enable" bit.

### Envelope Generator Control

To accomplish the generation of complex envelope patterns, two independent methods of control are provided: first, it is possible to vary the frequency of the envelope using registers R13<sub>g</sub> and R14<sub>g</sub>; second, the relative shape and cycle pattern of the envelope can be varied using register R15<sub>g</sub>. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control. (See Figure 1 and 2).

### Envelope Period Control (R13<sub>g</sub>, R14<sub>g</sub>)

The frequency of the envelope is obtained by first dividing the input clock by 256, then by further dividing the result by the programmed 16 bit Envelope Period value. This 16 bit value is obtained by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated:

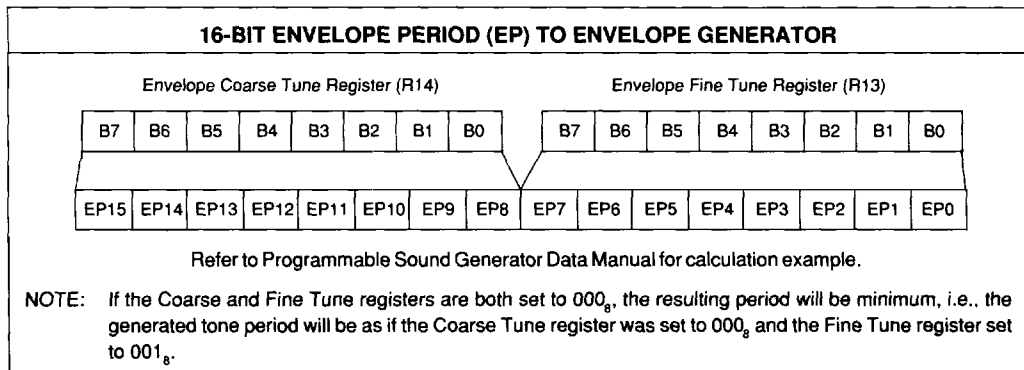


### Envelope Shape/Cycle Control (R15<sub>g</sub>)

The Envelope Generator further divides the envelope period by 16, producing a 16-state per cycle envelope pattern as defined by the 4-bit counter output, E3, E2, E1 and E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern of the 4-bit counter. (See Figure 4 and 5).

This envelope shape/cycle control is contained in the lower 4 bits (B3-B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated:

ENVELOPE SHAPE/CYCLE CONTROL BITS		
Bit	Signal	Function
0	HOLD	When this is set high (logic 1) the envelope is limited to one cycle, the value of the envelope at the end of the cycle being held.
1	ALTERNATE	When set high (logic 1) the envelope counter reverses direction at end of each cycle (i.e. performs as an up/down counter).
2	ATTACK	When set high (logic 1) the envelope counter will count up (attack). When set low (logic 0) the counter will count down (decay).
3	CONTINUE	When set high (logic 1) the cycle pattern will be defined by the HOLD bit. When set low (logic 0) the envelope counter will reset to 0000 after one cycle and hold that value.

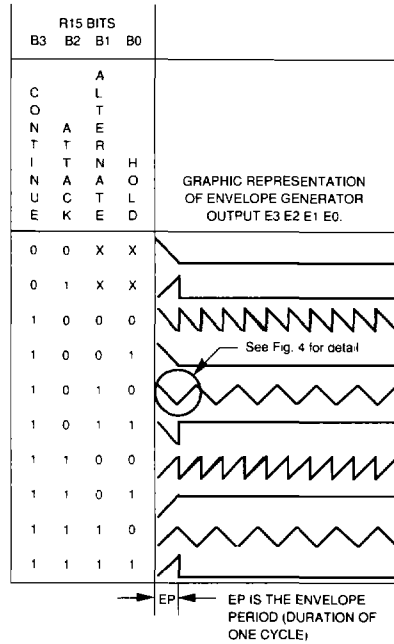


# AY38910A/AY38912A

## D/A Converter

Since the primary use of the PSG is to produce sound for the non-linear amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range from 0 to 1 volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4 bit outputs of the Amplitude Control block while the Mixer outputs provide the base signal frequency (Noise and/or Tone). (See Fig. 3).

**FIG. 1: ENVELOPE SHAPE /CYCLE OPERATION**



**FIG. 2: DETAIL OF TWO CYCLES**  
(ref. waveform "1010" in Fig. 1)

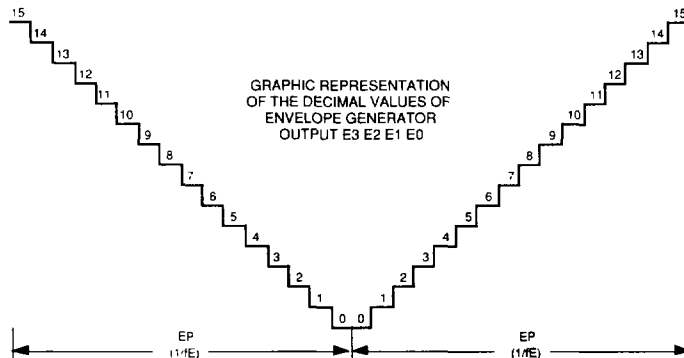
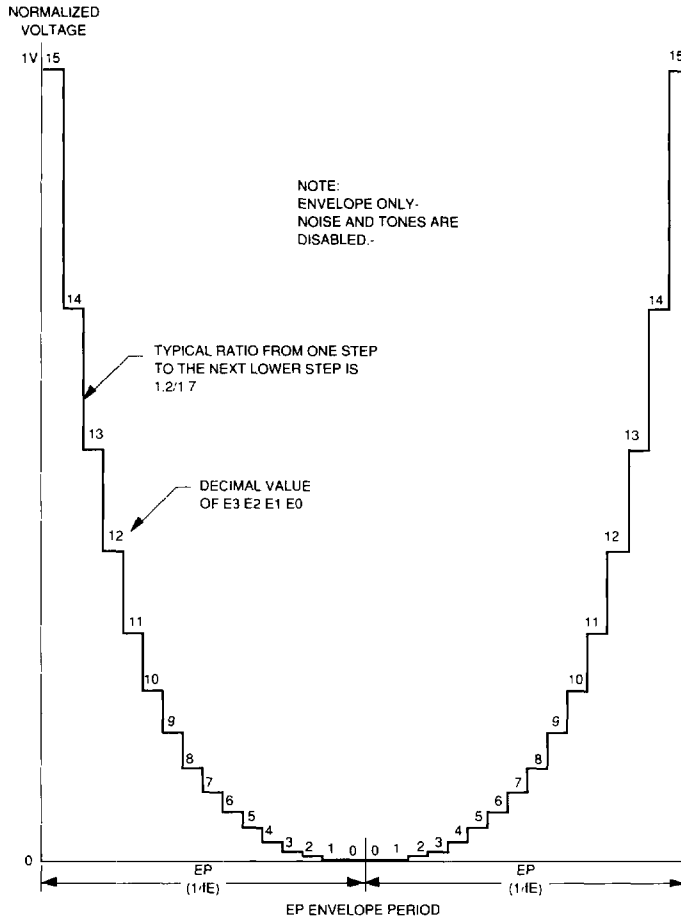




FIG. 3: D/A CONVERTER OUTPUT



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Fig. 4 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

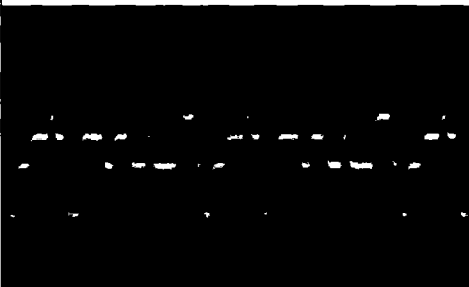


Fig. 5 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES



# AY38910A/AY38912A

## ELECTRICAL CHARACTERISTICS

### Maximum Ratings\*

Storage Temperature.....-55°C to +150°C  
 Operating Temperature.....0°C to +70°C  
 VCC and all other Input/Output  
 Voltages with Respect to VSS.....-0.3V to +8.0V

### Standard Conditions

VCC = +5V ± 5%  
 VSS = GND  
 Operating Temperature = 0°C to +70°C  
 (Unless otherwise noted)

\*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS	Sym	Min	Typ**	Max	Units	Conditions
<b>All Inputs</b>						
Low Level	V <sub>IL</sub>	-0.2	-	0.8	V	
High Level	V <sub>IH</sub>	2.2	-	V <sub>CC</sub>	V	
<b>Data Bus (DA7-DA0) Output Levels</b>						
Low Level	V <sub>OL</sub>	0	-	0.4	V	I <sub>OL</sub> = 1.6mA, 150pF
High Level	V <sub>OH</sub>	2.4	-	V <sub>CC</sub>	V	I <sub>OH</sub> = 100µA, 150pF
<b>Data Bus(DA7-DA0) Input Leakage</b>						
Input Leakage	I <sub>IAL</sub>	-10	-	10	µA	V <sub>IN</sub> = 0.4V to V <sub>CC</sub>
<b>Analog Channel Outputs</b>						
Output Volume	V <sub>o</sub>	0	-	60	dB	Test Circuits: Fig. 6
Power Supply Current	I <sub>CC</sub>	-	70	90	mA	
Max. Current (per channel)	-	0.4	2.0	-	mA	V <sub>OUT</sub> = 0.7V, Amplitude Control Set to F
<b>I/O Ports</b>						
Pull Up Current Low	I <sub>IL</sub>	20	-	200	µA	V <sub>IN</sub> = 0.4V, Outputs disabled
Pull Up Current High	I <sub>IH</sub>	10	-	100	µA	V <sub>IN</sub> = 3.5V
<b>- as Outputs (A7-A0, B7-B0)</b>						
Low Level	V <sub>OL</sub>	0	-	0.5	V	I <sub>IL</sub> = 1.6mA
High Level	V <sub>OHh</sub>	3.5	-	V <sub>CC</sub>	V	I <sub>OHh</sub> = 10µA See
	V <sub>OH1</sub>	2.4	-	V <sub>CC</sub>	V	I <sub>OH1</sub> = 85µA Note 1
<b>- as Inputs (A7-A0,B7-B0)</b>						
Low Level	V <sub>IL</sub>	0	-	0.8	V	
High Level	V <sub>IH</sub>	2.4	-	V <sub>CC</sub>	V	
<b>- A8 and Reset Input</b>						
Pull up Current	I <sub>I<sub>LP</sub>U</sub>	-10	-	-100	µA	V <sub>IN</sub> = 0.4V
	I <sub>I<sub>HP</sub>U</sub>	-10	-	-50	µA	V <sub>IN</sub> = 2.4V
<b>- A9</b>						
Pull down Current	I <sub>I<sub>HP</sub>D</sub>	10	-	100	µA	V <sub>IN</sub> = 2.4V
<b>- BC1,BDIR, Clock Inputs</b>						
Input Leakage	I <sub>ICL</sub>	-10	-	10	µA	V <sub>IN</sub> = 0.4V to V <sub>CC</sub>

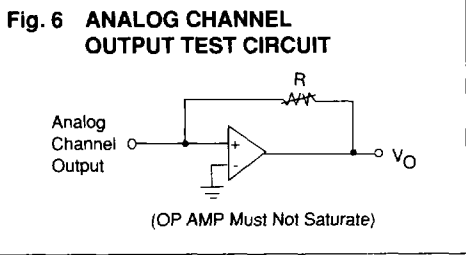
\*\*Typical values are at +25°C and nominal voltages.

Note 1: The active pull-up during an output operation will achieve a logic 1 of 2.4 volts in a time of typically 1 microsecond. However, from 2.4 volts to the high level of 3.5 volts the available pull up current will reduce significantly and further edge transition will be highly dependent upon load capacitance.

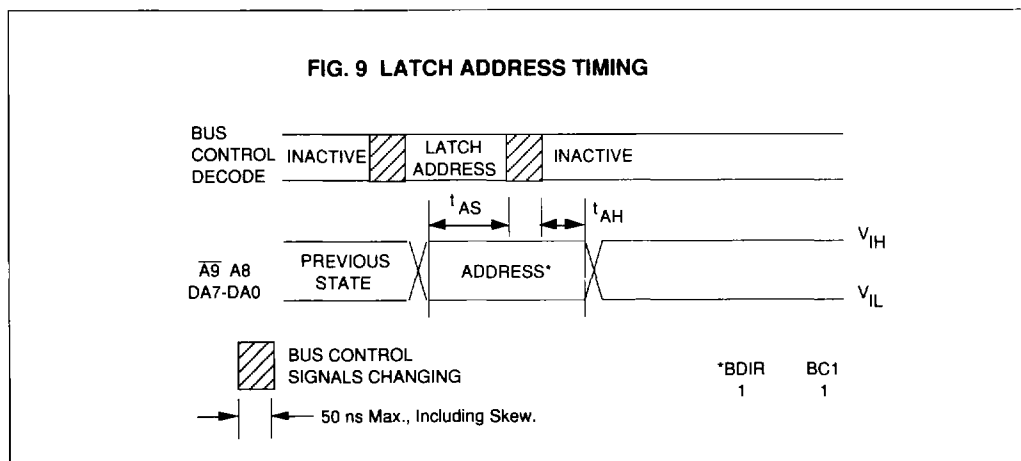
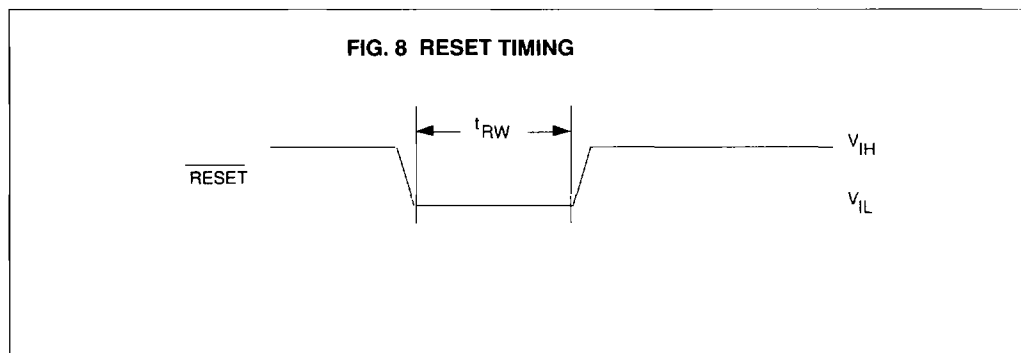
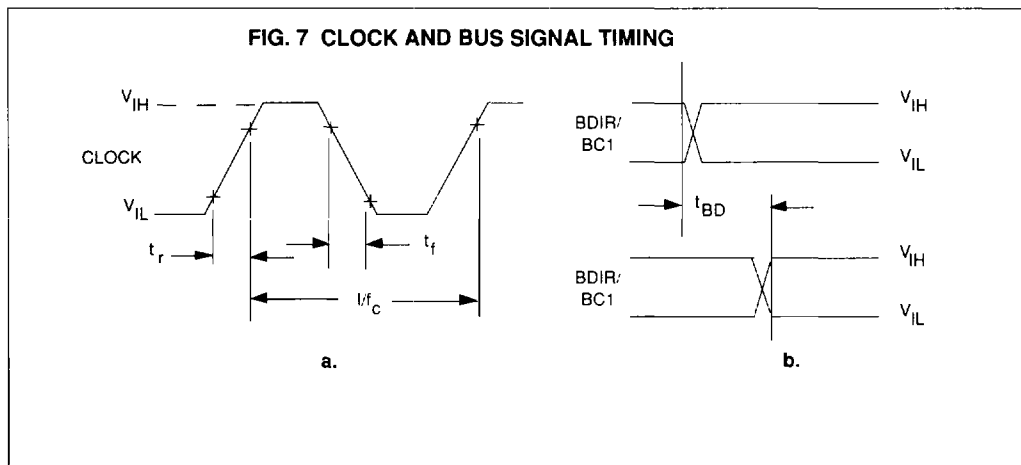
AC CHARACTERISTICS	Sym	Min	Typ**	Max	Units	Conditions
<b>Clock Input</b>						
Frequency	fc	1	-	2	MHz	Fig. 7
Rise Time	tr	-	-	50	ns	
Fall Time	tf	-	-	50	ns	
Duty Cycle	-	40	50	60	%	
<b>Bus Signals (BDIR, BC2, BC1)</b>						
Associate Delay Time	tBD	-	-	40	ns	
<b>Reset</b>						
Reset Pulse Width	trw	500	-	-	ns	Fig. 8
<b>A9, A8, DA7-DA0 (Address Mode)</b>						
Address Setup Time	tAS	300	-	-	ns	Fig. 9
Address Hold Time	tAH	65	-	-	ns	
<b>DA7-DA0 (Write Mode)</b>						
Write Data Pulse Width	tdw	500	-	10,000	ns	Fig. 10
Write Data Setup Time	tds	300	-	-	ns	
Write Data Hold Time	tdh	65	-	-	ns	
<b>DA7-DA0 (Read Mode)</b>						
Data Access Time from DTB	tdA	-	-	200	ns	Fig. 11
<b>DA7-DA0 (Inactive Mode)</b>						
Tri-state Delay Time from DTB	tTS	-	-	100	ns	
<b>I/O Ports (A7-A0, B7-B0)</b>						
Pull up Recovery Time	tPN	-	-	50	μsec	VOH = 3.5V CLOAD = 100pF See Note 2

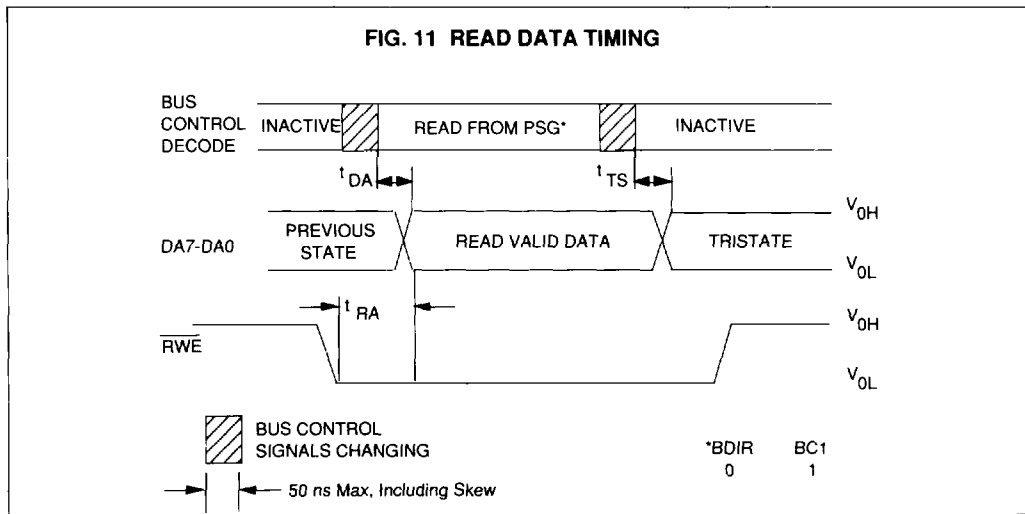
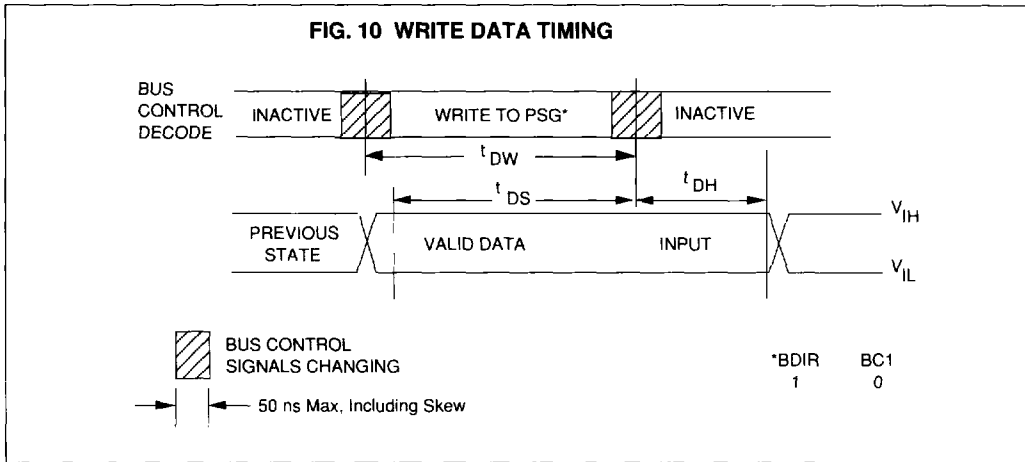
\*\*Typical values are at +25°C and nominal voltages

NOTE 2: Pull up recovery time is defined as the time required for any I/O pin A7-A0 or B7-B0 to change up to a 100pf capacitor load from 0.0 volts to 3.5 volts. This recovery time is conditional on the output function of Port A or Port B being deselected via Bits B7 and B6 of register R10.



## TIMING CONDITIONS FOR AC CHARACTERISTICS





# AY38910A/AY38912A

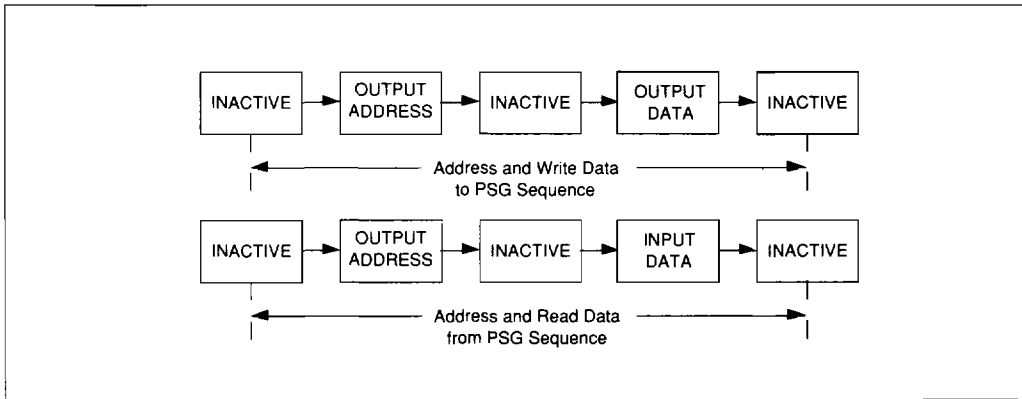
## TIMING DIAGRAMS

### State Timing

While the state flow for many microprocessors can be somewhat involved for certain operations, the sequence of events necessary to control the PSG is simple and straightforward. Each of the three major state sequences (Latch Address, Write to PSG, and Read from

PSG) consists of several operations (indicated below by rectangular blocks) defined by the pattern of bus control signals (BDIR, BC1).

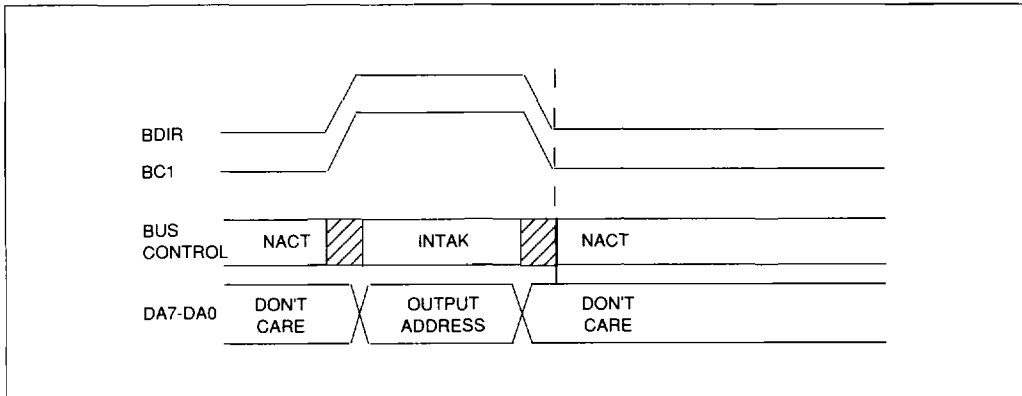
The functional operation and relative timing of the PSG control sequences are described in the following sections.



### Address PSG Register Sequence

The Latch Address sequence is normally an integral part of the write or read sequences but for simplicity is illustrated here as an individual sequence. Depending

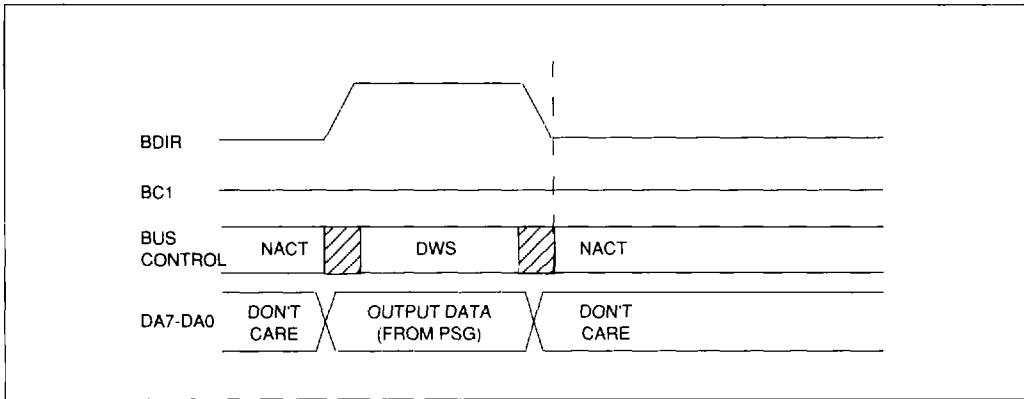
upon the processor used, the program sequence will normally require four principal microstates: (1) send NACT (inactive); (2) send INTAK (latch address); (3) put



**Write Data to PSG Sequence**

The Write to PSG sequence, which would normally follow immediately after an address sequence, requires

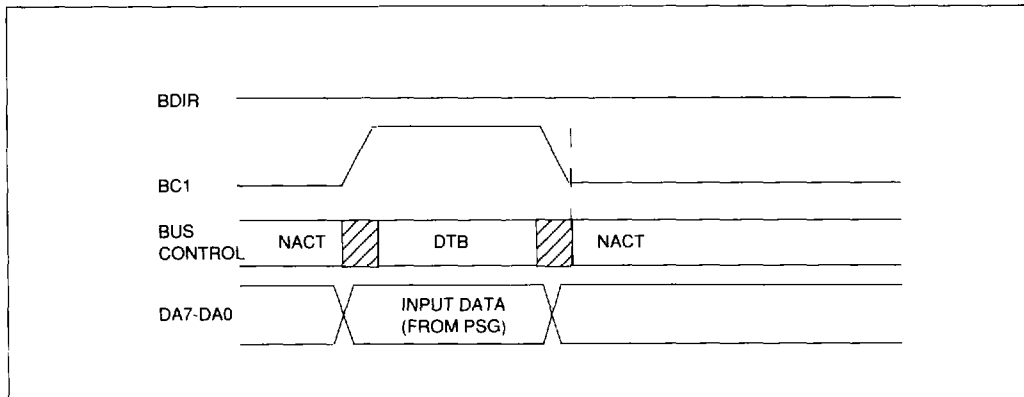
four principal microstates: (1) send NACT (inactive); (2) put data on bus; (3) send DWS (write to PSG); (4) send NACT (inactive).



**Read Data From PSG Sequence**

As with the Write to PSG sequence, the READ from PSG sequence would also normally follow immediately after an address sequence. The four principal microstates of

the read sequence are: (1) send NACT (inactive); (2) send DTB (read from PSG); (3) read data on bus; (4) send NACT (inactive).



# AY38910A/AY38912A

## SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

